REMARKS

This Amendment is submitted in response to the Examiner's Action mailed January 30, 2004, with a shortened statutory period of three months set to expire April 30, 2004. Claims 1-26 are currently pending. With this amendment, claims 1, 6, 9, 13, 15, 19, 21, and 25 have been amended.

The Examiner rejected claims 1-26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,633,916 issued to *Kauffman* in view of U.S. Patent 5,319,760 issued to *Mason*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

The claims have been amended to describe the feature of a 64-bit firmware component that eliminates virtual addresses and page translation rendering virtual address translation from a virtual address to a 64-bit address unnecessary. Examples of support for these amendments can be found in the specification at page 3, lines 17-21, and page 11, lines 3-17.

Claims 6, 13, 19, and 25 have been amended to describe a processor that includes a cache where the cache is not used when the address is cache-inhibited and is used when the address is not cache-inhibited. One example of support for this amendment can be found in the specification at page 11, line 18, through page 12, line 6.

Kauffman does not teach a 64-firmware component that eliminates virtual addresses and page translations rendering virtual address translation from a virtual address to a 64-bit physical address unnecessary. *Kauffman* teaches, at column 21, line 66, through column 22, line 11, that a modification may be used when an instance needs to be capable of running entirely within its private memory in a system were instances do not share memory. In this modification, an instance may need to be capable of mapping physical memory into its virtual address space. Thus, *Kauffman* suggests a system where virtual address translation is necessary.

As another example, *Kauffman* describes mapping the APMP database header at column 25, lines 26-31, and lines 40-54. These sections of the reference describe an initial virtual address of the APMP database. Therefore, again, *Kauffman* suggests a system where virtual address translation is necessary.

Applicant's claim 1 describes a plurality of hardware devices that each operate in a 64-bit mode; and a firmware component for virtualizing the hardware devices for interaction with the plurality of operating systems, where the firmware component is implemented using 64-bits, eliminates virtual addresses and page translations, and renders virtual address translation from a virtual address to a 64-bit physical address unnecessary. *Kauffman* does not describe, teach, or suggest a system that includes a firmware component for virtualizing the hardware devices for interaction with the plurality of operating systems, where the firmware component is implemented using 64-bits, eliminates virtual addresses and page translations, and renders virtual address translation from a virtual address to a 64-bit physical address unnecessary. *Kauffman* teaches a modification where an instance may need to be capable of mapping physical memory into its virtual address space, and teaches virtual addressing being used for addressing an APMP database. Thus, *Kauffman* describes a system that includes virtual addressing.

Because *Kauffman* teaches virtual addressing, *Kauffman* teaches away from Applicant's claims. Therefore, *Kauffman* does not render Applicant's claims unpatentable.

The Examiner states that *Kauffman* describes the features of Applicant's claims but fails to describe a firmware component that is implemented using 64-bits. The Examiner refers to *Mason* as adding this feature. Applicant's amended claims describe a firmware component for virtualizing the hardware devices for interaction with the plurality of operating systems, where the firmware component is implemented using 64-bits, eliminates virtual addresses and page translations, and renders virtual address translation from a virtual address to a 64-bit physical address unnecessary.

Mason teaches a CPU that executes a virtual memory management system that employs a translation buffer for caching recently used page table entries. Thus, *Mason* clearly teaches a system that uses virtual addressing. The Examiner appears to agree that *Mason* teaches virtual addressing. The Examiner states that *Mason* teaches "the format 76 of the virtual address asserted on the internal address bus 56 is shown" on page 3 of the Office Action. Because *Mason* teaches virtual addressing, *Mason* teaches away from Applicant's claims.

Applicant's claim 6 describes a determination that the address is cache-inhibited. One of the processors includes a cache. The cache is not used when the address is cache-inhibited and is used when the address is not cache-inhibited.

The combination of *Kauffman* and *Mason* does not describe, teach, or suggest a firmware component that eliminates virtual addresses and page translations, and renders virtual address translation from a virtual address to a 64-bit physical address unnecessary in combination with a determination that the address is cache-inhibited, where the processor includes a cache, and where the cache is not used when the address is cache-inhibited and is used when the address is not cache-inhibited.

Applicant's claim 9 describes virtualizing the 64-bit hardware resources using a firmware component that is implemented using 64-bits where the 64-bit firmware component eliminates virtual addresses and page translations, and renders virtual address translation from a virtual address to a 64-bit physical address unnecessary; receiving a request to perform an action; responsive to a determination that values associated with the request are 64-bit quantities, performing the request; and responsive to a determination that the values associated with the request are 32-bit values, zero extending the values to 64-bit quantitics and performing the request using the 64-bit quantities.

The combination of *Kauffman* and *Mason* does not describe, teach, or suggest a firmware component that eliminates virtual addresses and page translations, and renders virtual address translation from a virtual address to a 64-bit physical address unnecessary in combination with the steps of responsive to a determination that values associated with the request are 64-bit quantities, performing the request; and responsive to a determination that the values associated with the request are 32-bit values, zero extending the values to 64-bit quantitics and performing the request using the 64-bit quantities.

Both *Kauffman* and *Mason* teach systems that use virtual addressing. Both *Kauffman* and *Mason* teach away from Applicant's claims and are therefore not properly combined to render Applicant's claims unpatentable.

It is respectfully urged that the subject application is patentable over the cited art and is now in condition for allowance. The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 04.30.04

Respectfully submitted,

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